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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,728	11/06/2001	Mohammad A. Abdallah	42390P5943C	2359

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BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/005,728	ABDALLAH ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16,18,21-24 and 39-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23 and 24* is/are allowed.

6)☒ Claim(s) *16,18,21,22,39-41,43 and 44* is/are rejected.

7)☒ Claim(s) *42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 16, 18, 21-24, and 39-44 remain for examination.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. Claims 23-24 are allowable over the prior art of record.

4. Claim 42 is objected to as being dependent upon a rejected base claim, but would render the base claim allowable if bodily incorporated into the base claim such that the new base claim included all of the original limitations of the base claim, any intervening claims, and the objected claim.

5. Claims 39-41 are rejected under 35 USC 102(e) as being anticipated by Van Hook et al., U.S. Patent 5,734,874.

6. Claims 43-44 are rejected under 35 USC § 103 as being unpatentable over Van Hook et al. in view of Lee, U.S. Patent 5,721,697.

7. Claim 16 is rejected under 35 USC § 102(e) as being anticipated by Yung, U.S. Patent 5,996,066, or, in the alternative, under 35 USC § 103 as obvious over Yung in view of Van Hook et al.

8. Claim 18 is rejected under 35 USC § 103 as being unpatentable over Yung in view of Van Hook et al.

9. Claims 21-22 are rejected under 35 USC § 103 as being unpatentable over Yung in view of Van Hook et al. and further in view of Lee.

Van Hook et al., Lee, and Yung were cited as prior art references in paper number 20070529, mailed May 31, 2007.

10. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, paper number 20070529, mailed May 31, 2007.

11. Applicant's arguments filed February 29, 2008 have been fully considered but they are not deemed to be persuasive.

12. In the remarks, applicant argues in substance:

A. That: [as to claim 16] "The Examiner indicates that the "pixel distance" of Yung (col. 5

> lines 25-27) would be interpreted as the packed sum of absolute differences (PSAD) instruction and that the "single instruction [that] does both a multiply of two partitioned values, and an add with a separate, third value, with a masking capability," (col. 2 lines 10-14) would be interpreted as the packed multiply-add (PMAD) instruction.
>
> Applicant respectfully submits that one skilled in the art would distinguish at least between the multiply-accumulate with masking instruction of Yung and the claimed PMAD instruction. In fact Yung distinguishes between then (e.g. col. 6, line 51-53) saying that, "The result of the multiplication is added in an adder/subtracter 96 with a value from a register 98 (as opposed to adding together partitioned fields of the multiply result as done in the Intel MMX instruction)." (i.e. PMAD).

This is not found persuasive because while the examiner is fully cognizant of the fact that applicant's invention as described in the specification differs in significant ways from the disclosure of Yung, applicant's invention in the specification is not what is being rejected. It is applicant's overly broad claim language, which while covering their own disclosed invention, is of sufficient breadth that it also covers numerous other disclosures, such as that of Yung, which is being rejected.

> "It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).
>
> "The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

As is clear from applicant's arguments, applicant is reading into the claims a significant amount of detail which is not required by the claim language itself. I.e., note applicant's argument regarding Yung's multiply-accumulate instruction, where applicant argues that Yung has distinguished his disclosed instruction as different from the Intel (TM) MMX (TM) PMAD instruction. Applicant's claim 16 references the relevant instruction by the following language: "a packed multiply-add (PMAD) instruction having a second format to identify a second set of packed data". The quoted language is the sum total of the definition of "PMAD" in applicant's claim 16. This language does not provide sufficient claimed details of the "PMAD" operation to require that the claims be read as narrowly as applicant is reading them, i.e. as requiring the Intel (TM) MMX (TM) PMAD instruction.

> "limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." *Intervet Am.*,

v. Kee-Vet Labs., 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

At best, the sum total of the definition provided by applicant's claimed PMAD instruction is that it is an instruction which performs a packed multiply-add operation. **Any** instruction in the prior art which performs a packed multiply-add operation, no matter what internal operations are utilized to implement the "packed multiply-add" would anticipate this claim language. The only requirement to meet this claim language is that the operation be "packed", "multiply", and "add".

The Yung disclosure teaches just this requirement:

col. 6 lines 43-46: "Accordingly, the present invention provides a **single instruction** which **does both the multiply and add** (or subtract) operation utilizing separate operands."

col. 6 lines 47-48: "Register 92 could be a source register, **containing multiple partitioned pixel values.**"

As seen from the above two quotes from Yung's disclosure, a single instruction is taught that is "packed" ("multiple partitioned pixel values"), performs "multiply" ("does ... multiply") and performs "add" ("does ... add"). Therefore, no matter that applicant's disclosed invention differs significantly from the Yung disclosure, it is the fact that applicant has placed none of that difference into the claimed invention that the Yung disclosure anticipates the claimed invention.

> "The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

B. That: [in regards to claim 16] "Applicant further submits that Yung does not disclose enough to anticipate the PSAD instruction, but if one skilled in the art is presumed to understand the vis_pdist instruction of Sun Microsystems, Inc. then one skilled in the art would also distinguish between it and the claimed PSAD instruction."

This is not found persuasive because initially, applicant makes the unsupported assertion that one of skill in the art would distinguish between Yung and that which applicant has claimed, without articulating any reasoning for why applicant is asserting that position. Secondly, in the same manner as the description above regarding the PMAD instruction, what applicant has claimed versus what applicant has disclosed differ tremendously. Applicant's

sole claimed definition for the PSAD instruction consists of this text: "a packed sum of absolute differences (PSAD) instruction having a first format to identify a first set of packed data". Applicant is again arguing that the claim language contains significant additional limitations beyond that which is actually present in the claim language.

> "limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

The minimal amount of the invention that applicant has placed in the claims requires that the PSAD instruction be "packed" and perform a "sum of absolute differences". Any instruction disclosed in the prior art which is "packed" and performs a "sum of absolute differences" would anticipate this claim language. Yung as well also anticipates this overly broad claim language:

> Yung col. 5 lines 26-28 "At each dispatch, the PDU 46 may dispatch either a pixel distance computation instruction"

Yung does not further define the "pixel distance computation instruction", instead relying on the fact that one of skill in the art would have knowledge of what is meant by a "pixel distance computation instruction".

> MPEP 2163: "Information which is well known in the art need not be described in detail in the specification. See, e.g., Hybritech, Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1379-80, 231 USPQ 81, 90 (Fed. Cir. 1986)."

Accordingly, in the rejections, Van Hook et al. was utilized to show what was the well known definition of a "pixel distance computation instruction", which Van Hook et al. defines at col. 10 lines 53-64:

> Referring now to FIGS. 9a-9b, the pixel distance computation instructions, and the pixel distance computation circuit are illustrated. As shown in FIG. 9a, there is one graphics data distance computation instruction 138 for simultaneously accumulating the absolute differences between graphics data, **eight pairs** at a time. The PDIST instruction 138 subtracts **eight 8-bit graphics data in the rs1 register** from **eight corresponding 8-bit graphics data in the rs2 register**. The sum of the absolute values of the differences is added to the content of the rd register. The PDIST instruction is typically used for motion estimation in video compression algorithms."

As seen from the above quote of the Van Hook et al. disclosure, a "pixel distance computation

instruction" is an instruction that is "packed" ("eight pairs at a time", "eight 8-bit ... data ... from eight ... 8-bit ... data"), and performs a "sum of absolute differences" ("The sum of the absolute values of the differences"). Accordingly, Yung has disclosed, by relying on knowledge of the art, an instruction which is identical in every way to the minimal amount of applicant's invention that applicant has chosen to place into the claim language.

C. That: [in regards to claim 16] "Further, what Yung does disclose about the pixel distance instruction (e.g. Fig. 5, 56) is enough for one skilled in the art to determine that execution unit 28 (in Fig. 1; or 38 in Fig. 2; or execution unit 58 in Fig. 5) is not the same as execution unit 26 (in Fig. 1 or in Fig. 2; or execution unit 56 in Fig. 5) and does not perform both the first operation of the first set of operations initiated responsive to decoding the PSAD instruction and the second operation of the second set of operations initiated responsive to decoding the PMAD instruction, as claimed."

This is not found persuasive because applicant is mis-interpreting the teachings of Yung. Yung's fig. 2 is described as showing more detail of units 26 and 28 of fig. 1, with the exception that unit 28 of fig. 1 is referenced as 38 in fig. 2.

> Yung col. 4 lines 2-3: "FIG. 2 shows the floating point/graphics execution units 26 and 28 in more detail."

Further, Yung describes fig. 4 as showing internal detail of box 26 of figs. 1-2, and fig. 5 as showing internal details of box 28 of fig. 1 and box 38 of fig. 2:

> Yung col. 4 lines 37-39: "Referring now to FIG. 4, a block diagram illustrating the relevant portions of one embodiment of the first partitioned execution path in unit 26 is shown."
>
> Yung col. 5 lines 17-19: "Referring now to FIG. 5, a block diagram illustrating the relevant portion of one embodiment of the FP/graphics multiply unit 28 in further detail is shown."

As is clearly detailed by fig. 5, execution unit 28 of fig. 1 contains the pixel distance calculator (56). Therefore execution unit 28 of fig. 1 is clearly responsible for execution of the pixel distance instruction. It is also apparent that element 58 of fig. 5 within execution unit 28 of fig. 1 is the unit responsible for the packed multiply-add operation of Yung as well. This is because fig. 7, which details the packed multiply-add system, clearly shows that a multiplier is required to perform this operation. The only unit of units 26 and 28 of fig. 1 which contains a multiplier is unit 28 (see fig. 5, showing multiplier 58 contained inside unit 28 of fig. 1). Unit

26, detailed as fig. 4, does not contain a multiplier, but instead contains an adder, a logical unit, and merge/alignment unit. Accordingly, the only unit of fig. 1 which contains the necessary circuitry to perform a multiply-add is unit 28. As unit 28 is responsible for both the pixel distance instruction and the packed multiply-add instruction, Yung discloses one execution unit (unit 28 of fig. 1) which performs a first operation of the first set of operations and performs a second operation of the second set of operations as claimed in claim 16.

D. That: [in regards to claim 16] "Applicant respectfully submits that additional disclosure of PDIST (e.g. with regard to Fig. 9a) supports the assertion that one skilled in the art would distinguish between it and the claimed PSAD instruction.
Further, Figs. 2 and 5 of Yung and of Van Hook appear identical and to one skilled in the art, would establish that a single execution unit would not be expected to perform both the first operation of the first set of operations initiated responsive to decoding the PSAD instruction and the second operation of the second set of operations initiated responsive to decoding the PMAD instruction, as set forth in claim 16."

As to both these points above, they have been adequately treated in the prior pages and the discussion therein is hereby incorporated by reference.

E. That: [in regards to claim 39] "Van Hook discloses (col. 5, lines 11-17) that "At each dispatch, the PDU 46 may dispatch either a pixel distance computation instruction, or a graphics data compare instruction to the second partitioned execution path 34. The pixel distance computation circuit 56 executes the pixel distance computation instruction."
Thus one skilled in the art would determine that the PDU 46 does not anticipate the claimed decode logic to initiate the three claimed operations responsive to decoding the PSAD instruction, but simply dispatches the PDIST instruction of Van Hook."

This is not found persuasive because the dispatching of the PDIST instruction in Van Hook et al. causes execution of the PDIST instruction to occur. Such execution of the PDIST instruction causes the operations defined for the PDIST instruction to happen. Therefore, the dispatching of the PDIST by PDU 46 "initiates" (i.e., starts, begins, causes to happen) the operations defined for the PDIST instruction. The fact that the operations match the claimed operations will be explained below.

F. That: [as regards to claim 39] "Thus from Fig. 9b of Van Hook and the above disclosure, one of skill in the art may conclude that Van Hook performs the second known technique (2) rather than the claimed PSUBWC operation and the PABSRC operations.
The Examiner claims that subtracters 57a-57h write carries, and that multiplexers 59a-59h read carries, but Applicant respectfully finds no storage elements, to which carries may be written, or from which carries may be read, consistent with

> what would be understood from the claimed PSUBWC operation and the PABSRC operations by one skilled in the art in the content of the entire patent including the specification."

This is not found persuasive because applicant is again reading into his overly broad claim language a significant amount of limitations from the specification beyond that which is necessary for understanding the claims.

> "limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

> "it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

Applicant's claimed definition for the two argued limitations "PSUBWC" and "PABSRC" are the following two lines:

> "a packed subtract and write carry (PSUBWC) operation" (claim 39 line 7)
> "a packed absolute value and read carry (PABSRC) operation" (claim 39 line 8)

These two lines amount to the sum total of applicant's definition in the claims as to the meaning of the two operations. The first operation "PSUBWC" requires "packed", "subtract", and "write carry". The second operation "PABSRC" requires "packed", "absolute", and "read carry". Looking to Van Hook et al.'s fig. 9b, one sees "packed" ("byte slice 0" ... "byte slice 7") and therefore the "packed" requirement of the claims is met for both operations. Additionally, one finds "subtract" ("8 bit subtract") and accordingly the "subtract" requirement of the PSUBWC operation is met. One further finds absolute value (elements 57a-59a through 57h-59h perform an absolute value operation, see col. 10 lines 61-62: "The sum of the absolute values of the differences is added to the content of the rd register." Therefore the "absolute value" requirement of the PABSRC operation is met.

As to applicant's argument regarding the "write carry" and "read carry" limitation, initially it should be pointed out that applicant's claims do not recite any storage for the

carries. Accordingly, applicant's argument that Van Hook et al.'s fig. 9b does not disclose storage is not well founded because applicant's claims require no such storage.

> "The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).
>
> "limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989)(citation omitted).

Additionally, as seen from fig. 9b of Van Hook et al., the first subtracters (57a ... 57h) each have a carry output (the line from the subtracter to the muxes 59a ... 59h). So, the muxes 59a ... 59h are "reading carries" because they "read" the input value on their respective input line connecting them to the subtracters 57a ... 57h. Therefore, the "read carry" part of the PABSRC operation is met by Van Hook et al. in fig. 9b. Additionally, as seen from fig. 9b, the subtracters 57a ... 57h "write carries" because they "write" their respective carry output from the subtract operation onto the line connecting the subtracters with the muxes (59a ... 59h). Therefore, the "write carry" part of the PSUBWC operation is also met by Van Hook et al.'s fig. 9b. Accordingly, Van Hook et al. does indeed disclose that which applicant is claiming.

G. That: [in regards to the combination of Van Hook et al. and Lee] "Thus without a suggestion to modify Van Hook, it must be assumed that the combination results from impermissible hindsight using Applicant's own disclosure."

This is not found persuasive because it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Lee's teachings into a system containing the teachings of Yung or Van Hook et al. because of Lee's teachings that the conventional manner of performing a tree addition is to perform plural operations over many cycles which consequently consumes a lengthy amount of time (col. 1 lines 29-35). Lee provides a system for performing a tree add operation in fewer cycles with only minor changes to an existing multiplication circuit (col. 2 lines 1-2) for the purposes of accelerating graphics operations (col. 1 lines 20-29 and 36-40). As both Yung and Van Hook et al. are directed to

accelerating graphics operations (Yung col. 1 line 65 to col. 2 line 2, Van Hook et al. col. 2 lines 6-11) there is a connective nexus between the three references that would motivate one of skill in the art to combine their respective teachings. Additionally, as Van Hook et al. in fig. 9b is performing a tree addition (adders 61a ... 61c perform a tree addition) the teachings of Lee are particularly relevant to the disclosure of Van Hook et al.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

/Richard Ellis/
Primary Examiner, Art Unit 2183
April 3, 2008